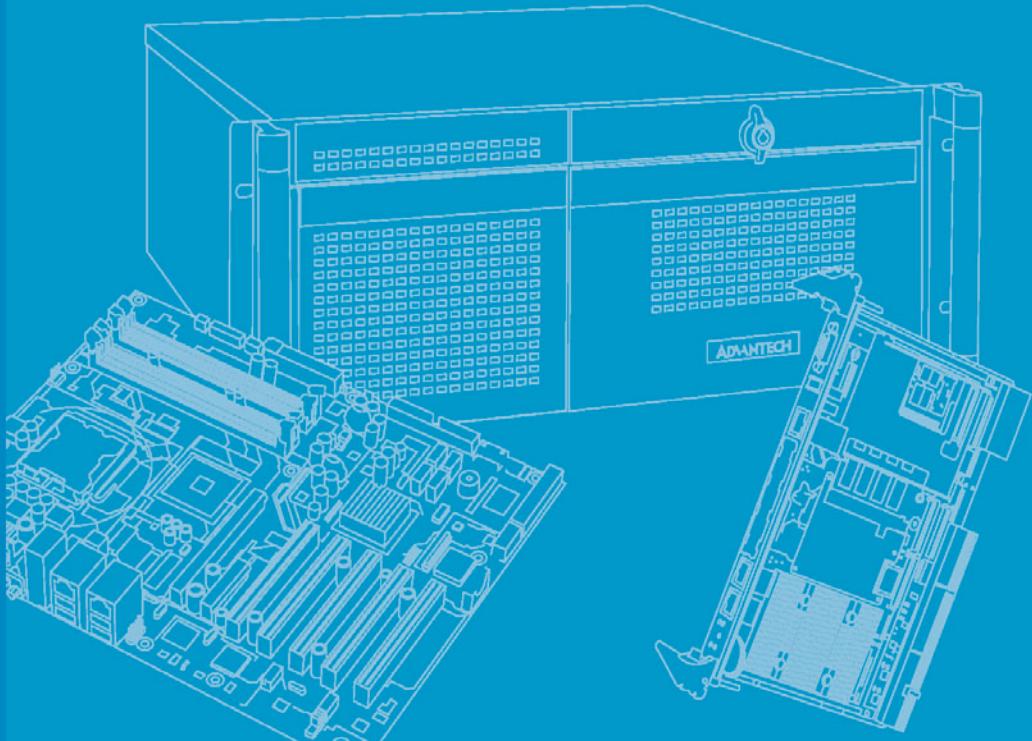


User Manual



UTCA-5503

MicroTCA™ Carrier Hub

Trusted ePlatform Services

ADVANTECH

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 - Description of your software (operating system, version, application software, etc.)
 - A complete description of the problem
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Caution! *Cautions are included to help you avoid damaging hardware or losing data. e.g.*



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Note! *Notes provide optional additional information.*



Document Feedback

To assist us in making improvements to this manual, we would welcome comments and constructive criticism. Please send all such - in writing – to:
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Packing List

- UTCA-5503 MicroTCA Carrier Hub x1
- User manual (PDF file) CD-ROM disc x1
- Warranty certificate document x1
- Safety Warnings: CE, FCC class B

If any of these items are missing or damaged, contact your distributor or sales representative immediately.

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1. Read these safety instructions carefully.
2. Keep this User Manual for later reference.
3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.
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7. The openings on the enclosure are for air convection. Protect the equipment from overheating. **DO NOT COVER THE OPENINGS.**
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13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If one of the following situations arises, get the equipment checked by service personnel:
 - The power cord or plug is damaged.
 - Liquid has penetrated into the equipment.
 - The equipment has been exposed to moisture.
 - The equipment does not work well, or you cannot get it to work according to the user's manual.
 - The equipment has been dropped and damaged.
 - The equipment has obvious signs of breakage.
15. **DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -20° C (-4° F) OR ABOVE 60° C (140° F). THIS COULD DAMAGE THE EQUIPMENT. THE EQUIPMENT SHOULD BE IN A CONTROLLED ENVIRONMENT.**
16. **CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER, DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.**
17. The sound pressure level at the operator's position according to IEC 704-1:1982 is no more than 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.
- Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.

Product Configurations

Table 1.1: Product Configurations

Model Number	MCMC	LAN1 RJ45	LAN2 RJ45	LAN2 SFP	Fabric A GbE Switch	Comments
UTCA-5503-0000E	✓	✓	-	-	-	Management only, no switch
UTCA-5503-1000E	✓	✓	✓	-	✓	Management and switch
UTCA-5503-2000E	✓	✓	-	✓	✓	Management and switch

We Appreciate Your Input

UTCA-5503 is a new product based on new technology. Please let us know of any aspect of this product, including the manual, which could use improvement or correction. We appreciate your valuable input in helping make our products better.

Glossary

AMC	Advanced Mezzanine Card
CPU	Central Processing Unit
CU	Cooling Unit
FPGA	Field-Programmable Gate Array
FRU	Field Replaceable Unit
GbE	Gigabit Ethernet
I2C	Inter-Integrated Circuit, 2-wire serial bus
IPMB	Intelligent Platform Management Bus, I2C type
IPMI	Intelligent Platform Management Interface
Mb	Mega-bit
MCH	MicroTCA Carrier Hub
MCMC	MicroTCA Carrier Management Controller
Mgmt	Management
MII	Media Independent Interface
MLAN	Management LAN
OOS	Out OF Service
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PM	Power Module
SerDes	Serializer/Deserializer
SFP	Small Form-Factor Pluggable
ShM	Shelf Manager
SMA	SubMiniature version A
SGMII	Serial Gigabit Media Independent Interface
SRIO	Serial Rapid I/O
uShM	MicroTCA Shelf Manager
uTCA	MicroTCA
XAUI	10 Gigabit Attachment Unit Interface

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Chapter 1

Board Specification

1.1 Technical Data

Table 1.1: Advantech UTCA-5503 MCH Technical Data

MCH module	Standard MCH module (PCB Level 1), single width, full size		
Application/Security Processor	Optional on PCB Level 3		
Serial Interface	COM1 exposed to front panel as USB Slave interface through onboard USB/Serial converter, USB1.1 compliant		
Ethernet	<ul style="list-style-type: none"> ▪ 10/100BT Management LAN on Front panel (RJ45, labeled as LAN1, which may also be 10/100/1000BT Fabric LAN when MLAN is routed through base fabric switch) ▪ 10/100/1000BT Fabric LAN on Front panel (RJ45, labeled as LAN2) ▪ SFP Socket Fabric LAN on Front panel (alternative option) <ul style="list-style-type: none"> ▪ 1000BX GBE base fabric interface to backplane (12x) ▪ 1000BX GBE update channel to other MCH ▪ Management LAN may be routed through base fabric switch (option) ▪ Front panel ports may be routed over PCB Level 3 ▪ SGMII Interface from PCB Level 3 into base fabric switch 		
Extension Capabilities	Through backplane/PCB Level 2...PCB Level 4		
System Management Controller	<ul style="list-style-type: none"> ▪ Renesas H8S/2166 based microcontroller as MCMC ▪ Pigeon Point System based firmware solution ▪ Carrier manager ▪ Shelf manager (by default); optional to exclude uShM 		
Watchdog	A programmable watchdog is implemented in MCMC		
GbE switch controller	Two Marvell 88E6185 gigabit Ethernet switches		
GbE PHY	Two Marvell 88E1111 single-port gigabit Ethernet transceivers		
10/100 Ethernet MAC/PHY	One SMSC LAN9115 Ethernet controller		
FPGA	One Lattice LFXP6C programmable device		
SRAM	One Renesas M5M5V216ATP-55HI 2Mb static RAM		
Flash memory	One Macronix MX29LV160CBTC-70G 16Mb flash memory		
Power consumption	3.3 V	70 mA (max.), 42 mA (60% max.)	Mgmt power
	12 V	1000 mA (max.), 600 mA (60% max.)	Input voltage
Environmental conditions	Temperature and humidity (operating)		GR-63-CORE, Issue 3, R4-6
	Temperature and humidity (non-operating)		IEC60068-2-1, IEC 60068-2-3, IEC 60068-2-2
	Altitude		GR-63-CORE, Issue 3, R4-8 4-9, 4-10, O4-11,O4-12
	Vibration (operating)		IEC 60068-2-64
	Vibration (non-operating)		IEC 60068-2-6
	Shock (operating)		IEC 60068-2-27
	Shock (non-operating)		IEC 60068-2-27

Table 1.1: Advantech UTCA-5503 MCH Technical Data

Safety and others	UL94V0, RoHS
EMC	<ul style="list-style-type: none"> ▪ FCC class B ▪ >3dB margin targeted for single board within system
Standards compliance	PICMG MicroTCA.0 rev1.0, PICMG AMC.0 rev2.0, PICMG AMC.3 rev1.0, IPMI v1.5 rev1.1, IPMB communication protocol rev1.1

1.2 Advantech UTCA-5503 Features

1.2.1 MCMC

The MCMC on UTCA-5503 is built based on Pigeon Point Systems' (PPS) hardware/software reference design kit for MCMC.

1.2.1.1 H8S Microprocessor

Renesas Technology's HD64F2166 (referenced hereafter as the H8S) is used as the microcontroller for the MCMC implementation on Advantech's MCH (aMCH). This microcontroller contains a Renesas' H8S/2000 CPU as its core architecture, in addition to peripheral functions. The H8S is a highly integrated microcontroller that has on-chip Flash and SRAM memories. The peripheral functions of the H8S used in the aMCH MCMC design include the I2C controllers, free-running timer, watchdog timer (WDT), Serial Communication Interface (SCI), Low Pin Count (LPC) interface, Analog-to-Digital Converter (ADC), and GPIO. The LPC interface is optional for the implementation of the to-be-developed PCB Level 3 or PCB3 for short.

1.2.1.2 IPMB and I2C Implementations

The MCMC has six hardware I2C controllers, which are used as listed below.

Table 1.2: H8S I2C Bus Assignment

MCMC I2C	Used for
0	Carrier FRU I2C
1	reserved
2	IPMB0-A
3	IPMB0-B
4	MCMC private I2C
5	Radial IPMB / MCH Crossover IPMB

1.2.1.3 MCH to MCH Communication

At the moment of this manual creation, MCH redundancy is not supported by PPS. Consequently, to avoid potential damage, two MCH modules should not be used in one system until a firmware update with the PPS MCH redundancy feature is made available.

The two MCH's are linked through a crossover communication channel which may include any of the following interfaces:

- a crossover IPMB bus
- a full duplex crossover interface with differential I/O's (Xover 0, 2)
- a half duplex crossover interface with differential I/O's (Xover 1).
- a Fabric A update channel

While the later interface is for linking the fabric interfaces of the MCH's, the other three interfaces are for communication and redundancy & failure management. The protocol on these interfaces is not available in the uTCA specification and is implementation specific.

1.2.1.4 Thermal Sensor

Two LM75 thermal sensors are placed on opposite sides and differing locations of the PCB to monitor the ambient air temperature across PCB1 on UTCA-5503.

1.2.2 FPGA

An FPGA is used to integrate MCMC related glue logic, GPIOs, a UART and other interfaces. It will also hook up to the optional LPC bus to the Fabric Extension Connector (for a fabric extension module on PCB3). It may be used to connect FPGA resources to an optional processor on PCB3. A Lattice LXFP6 device is used to implement the FPGA.

1.2.3 RTC

The RTC is attached to the private I2C bus of the MCMC. It provides time of day and calendar function for the MCMC.

1.2.4 Base Fabric/Gigabit Ethernet

The overall Ethernet implementation on UTCA-5503 can be illustrated by the following diagram. Two Marvell 88E6185 switches are used to fulfill the following connections.

- 12 SERDES interface connections to AMCs on the uTCA backplane.
- 1 SERDES interface connection to the update channel of the other MCH on the uTCA backplane.
- 1 SGMII interface to fabric modules on PCB3.
- 1 SGMII interface to a GbE PHY device that may drive a 10/100/1000BT interface on the front panel. The RJ45 on the front panel may also be used to connect to the management LAN interface of the MCMC.
- 1 SGMII interface to a GbE PHY device that may drive another 10/100/1000BT interface or a SFP socket on the front panel.
- 1 Reverse MII interface for connection to the MCMC management LAN controller.

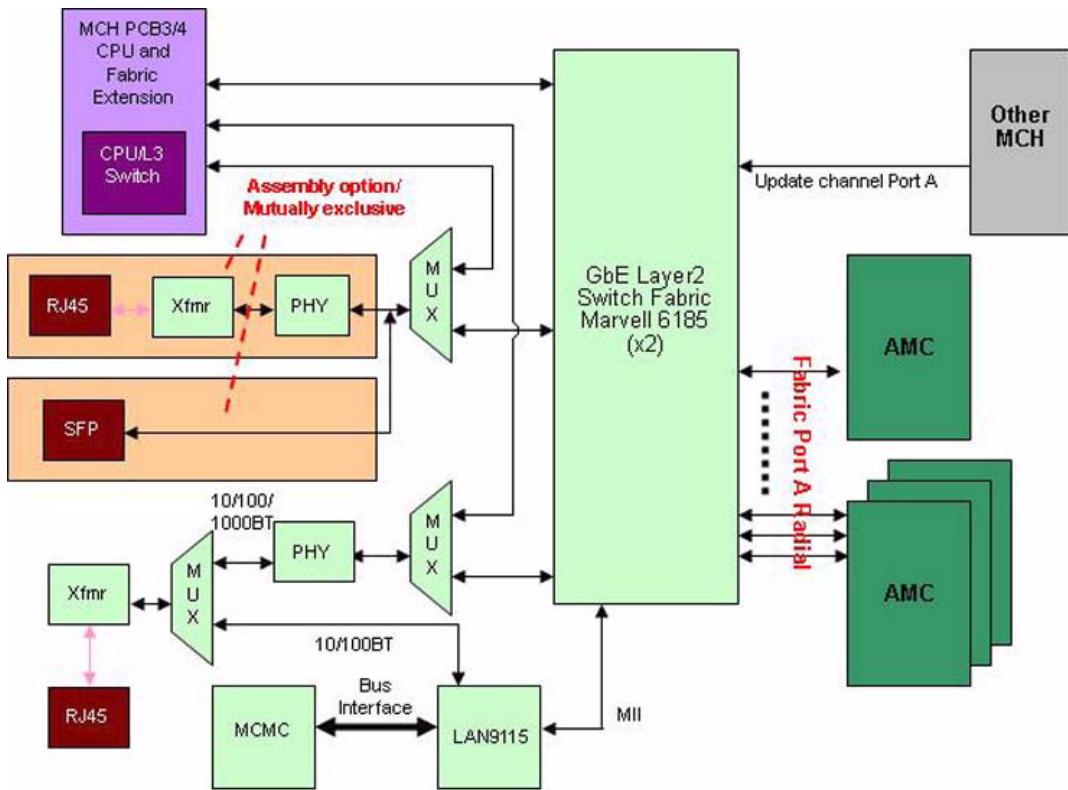


Figure 1.1 GbE architecture

The PHY's may be connected to a CPU or Layer 3 switch on PCB3 instead of a connection to the switch on PCB Level 1 (or PCB1).

1.2.4.1 Gigabit Ethernet Management and E-Keying

The basic UTCA-5503 supports unmanaged GbE operation only. Any managed GbE switch operation can only be supported by a CPU on PCB3. However, the MCMC on PCB1 will control the E-keying and disable/enable ports of the GbE switches accordingly. To support this, the switches are operated in a mode that allows the backplane ports to come up in a disabled state after reset. The MCMC microcontroller has access to the switch registers through a switch dependent interface, which is implemented in the FPGA. An EEPROM based configuration of the switch is supported for optional implementations without MCMC where the switch is auto-configured and acts as a purely unmanaged GbE switch.

To support managed applications driven by a CPU on PCB3, the FPGA is also hooked up to a LPC bus providing shared access to the switch management interface to both the MCMC and the PCB3 CPU. In this configuration, the MCMC will communicate the E-keying information to the PCB3 CPU over the LPC Bus or a UART interface.

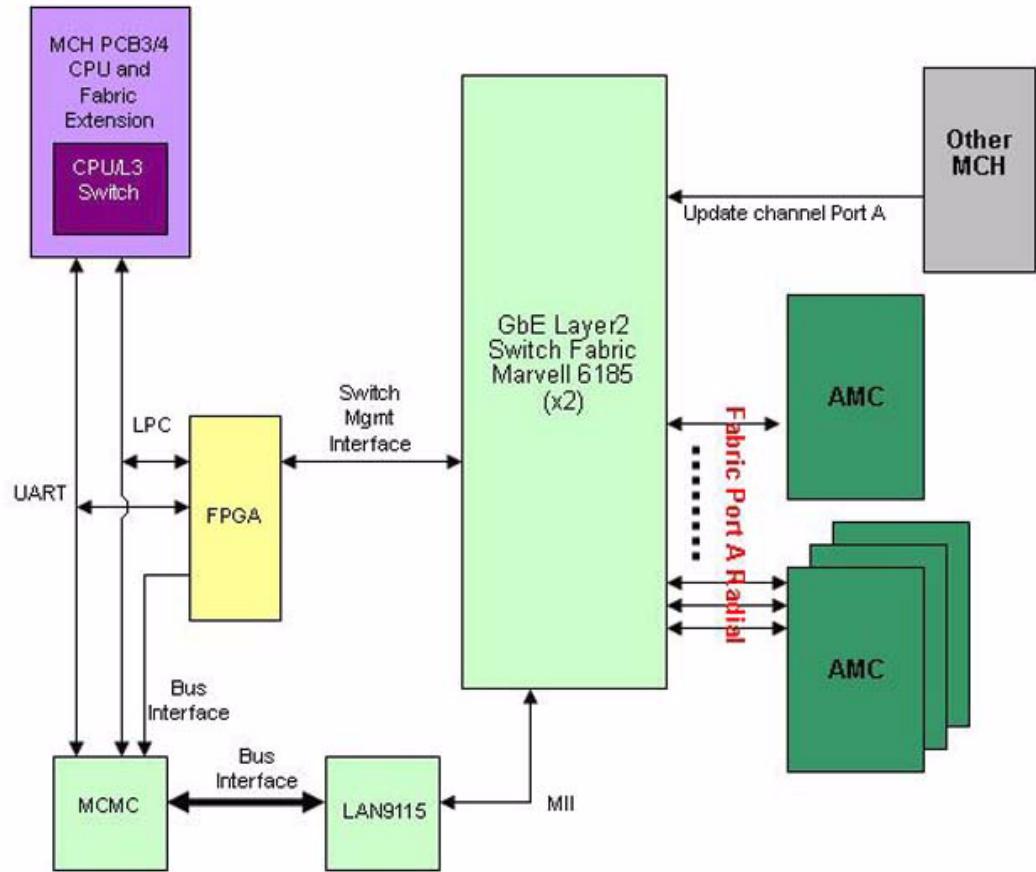


Figure 1.2 GbE Switch Management and E-keying

1.2.4.2 Gigabit Ethernet PHYs

Two Marvell 88E1111 PHY's are used. These PHY's support two different MAC interfaces: SGMII and RGMII. The SGMII interface is connected to the GbE switch and the RGMII interface will be connected to PCB3. Either selection of the two interfaces can be configured manually through IPMI command by the user when PCB3 is detected. This option is a static configuration that will not be changed during run time. Each of the PHY's is connected to a 10/100/1000BT copper interface. The use of a 2nd PHY is optional and mutual exclusive with the SFP port option (as shown in Figure 1.1).

1.2.4.3 SFP Port

A standard SFP port is provided as alternate assembly option instead of a 2nd RJ-45 connector. Standard SFP's are supported. The SFP will be directly connected to the GbE switch fiber port. To support auto configuration and management, the presence detect signal from the SFP is connected to the FPGA.

1.2.4.4 Management LAN Controller

An SMSC LAN9115 10/100Mbit Ethernet controller is connected to the MCMC bus interface to provide a management LAN interface. The LAN9115 contains an integrated 10/100BT PHY which may be used on the 1st RJ45 on the front panel as discussed above. Alternatively, the LAN9115 supports a MII interface which is connected to the GbE switch's Reverse MII interface. This interface is provided as an option to support routing management LAN traffic through the GbE switch fabric. Note that the implementation for this option is through jumper setting. A selection between the two options shall be a static configuration chosen at power up of the module.

1.2.5 USB Slave Interface

A full speed USB1.1 compliant slave port is implemented on a standard USB Type mini-B connector on the front panel. The implementation uses a standard USB host to a serial port converter chip which is cross-connected to the FPGA that implements a MUX to either connect the UART port to the H8S Serial Debug Interface, the H8S Command Line Interface or to a CPU on PCB3. The USB port can be used for debugging, diagnostic information and implementation of a serial console interface.

1.2.6 Clock Module Extension

A 20-pin connector is used for attaching a clock module on a to-be-developed PCB Level 2 (or PCB2) to the aMCH. The clock module has a tongue connector to the backplane. The purpose of the mezzanine module is to support clock buffering and distribution in an uTCA system. Furthermore, the aMCH supports one differential input and one differential output to PCB3 (Fabric Extension Module) as well as one differential and one single ended clock input from the Clock IO module and one differential clock output to the Clock IO module. Application of the clocks connected to PCB3 is reference clock distribution for fabric interface switches, especially in spread spectrum environments which are common in PCIe applications. Application of the clocks connected to the Clock IO module (PCB2) is multi-carrier/shelf synchronization and clock distribution as well as external reference clock reception such as GPS derived clocks or BITS clocks. For applications requiring lower accuracy and stability, the square wave output of the RTC on PCB 1 is also connected to the clock module.

The clock module is connected to the MCMC's private I2C bus and implements a FRU EEPROM on this bus. It is also connected to the I2C_ALARM interrupt line to the MCMC.

1.2.7 Clock I/O / Alarm Module Extension

The aMCH can also support another extension module on the to-be-developed PCB2: the ClockIO/ Alarm module. This module will have access to the front panel. As the name indicates, this extension socket can accept two kinds of modules: a ClockIO module or an Alarm Module.

The function of the ClockIO module is to provide front panel connectivity, basic signal buffering, and protection to external clocks. And, the Alarm module can carry a minimum set of Telco style Alarm circuitry.

1.2.8 Fabric Extension Module

The fabric extension module can be implemented on the to-be-developed PCB3. Its purpose is to provide fat pipes switching capabilities for protocols such as PCIe, XAUI, SRIO amongst others. Moreover, application processors can also be supported on PCB3. For example, an application processor on PCB3 can be used to create a firewall between the outside world's LAN and the internal base fabric on the uTCA backplane.

Chapter 2

**Applications and
Overview**

The MCH is a key element of the uTCA architecture (see Figure 2.1). It is used in uTCA systems and applications to provide

- carrier / shelf system management
- switching capabilities for the basic fabric interface (“common options”)
- clock distribution
- Fat pipes fabric switching capabilities

For details of the uTCA architecture, refer to PICMG® MicroTCA.0 R1.0, Micro Telecommunications Computing Architecture specification.

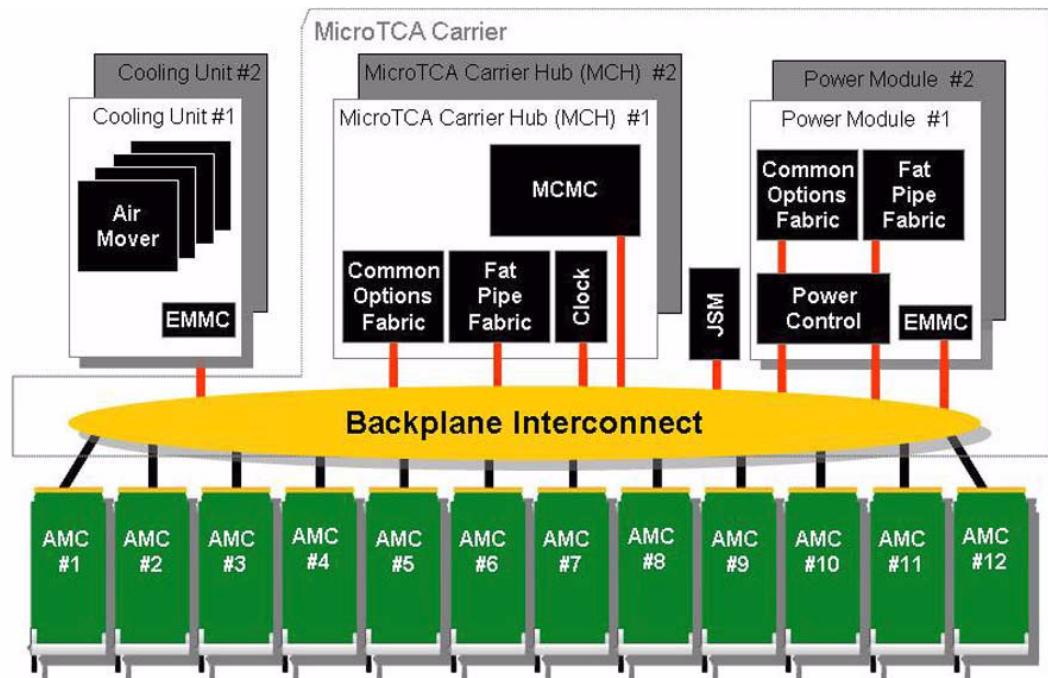


Figure 2.1 uTCA System Elements

2.1 Mechanical Basics

The MCH consists of a stack of 4 PCB layers, labeled as PCB1 to PCB4 as shown in Figure 2.2.

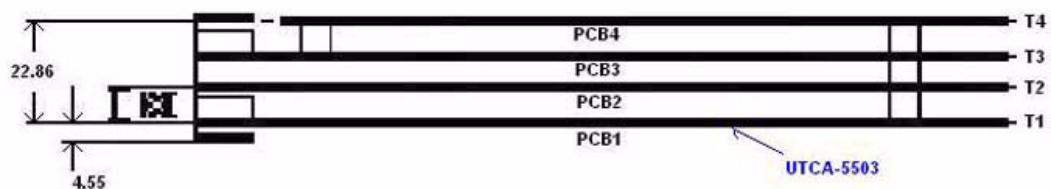


Figure 2.2 MCH PCB Naming Conventions

UTCA-5503, implemented on PCB1 of Advantech’s MCH, contains the basic features that every MCH must support as well as interface connections to PCB2 to PCB4.

- the management controller called the MCMC
- the common options switch fabric

All other PCBs except for PCB1 are optional for an MCH.

PCB2 carries the system clock logic and may also contain switching logic for fabric B which is normally used for SATA/SAS functionality on AMC modules. SATA is normally used for direct connection of a processor AMC and a SATA drive. Therefore, PCB2 with SAS/SATA functionality may just be implemented on custom request.

PCB3 contains switching logic for the fat pipes region as does PCB4. Because of component height limitation on PCB4 this PCB is just implemented as a bare backplane connection and will not carry active components.

2.2 System Management

UTCA-5503 implements both the Carrier Manager and Shelf Manager of a uTCA system. It may or may not be connected to an external System Manager as shown below.

The MCH connects to the AMC slots of an uTCA system with a radial IPMB according to IPMI and ATCA/AMC specifications. It senses the “presence detect” signals of each AMC slot (PS1#) and controls payload power for each slot by the ENABLE# signal. A redundant I2C bus is used for managing centralized system resources like the cooling units, power modules and carrier FRU devices. Connection to the outside world is implemented by either a dedicated front panel 10/100BT Ethernet interface or optional connection to the base fabric switch, in which mode the front panel interface will become a 10/100/1000BT fabric LAN connection. The system management functions are implemented on a microcontroller system referred to as the “MCMC”.

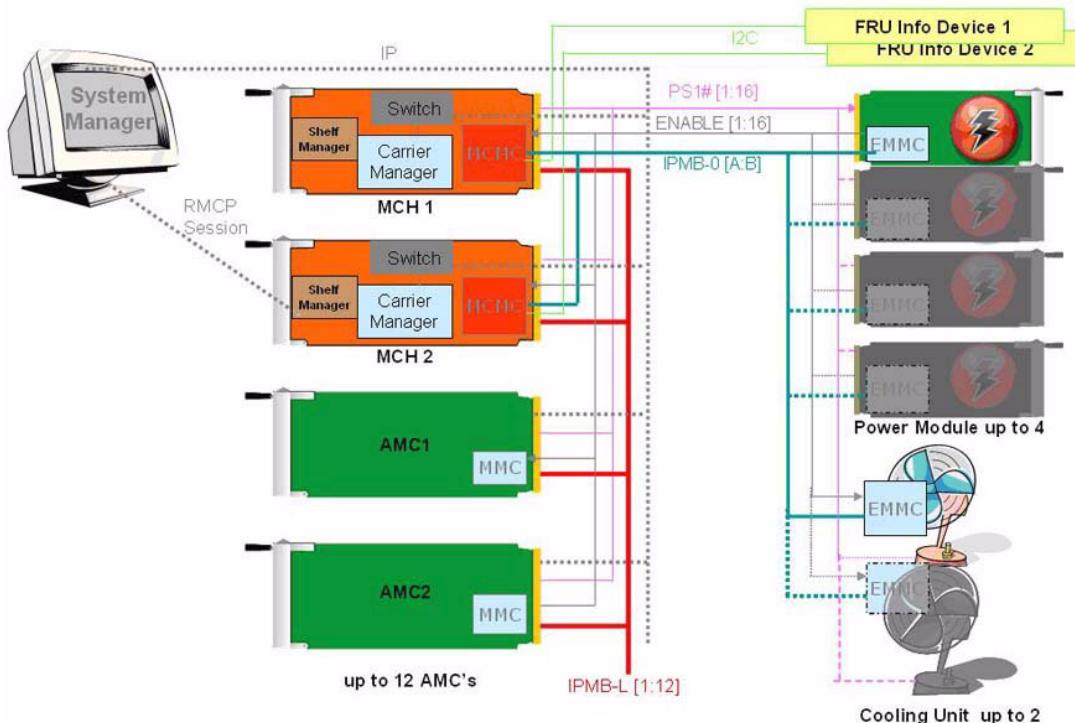


Figure 2.3 uTCA System Management Architecture

2.3 Clocks

A MCH may support clock distribution for up to 3 clocks per module. Each AMC slot supports two clock inputs (MCH to AMC), CLK1/3, and one clock output (AMC to MCH), CLK2. All clocks use LVDS compliant drivers/receivers. UTCA-5503 supports two different clock architectures, redundant and non-redundant as shown below. The redundant implementations are for dual MCH systems, and the non-redundant are for single MCH systems. This requires the implementations of different backplanes for non-redundant and redundant architectures.

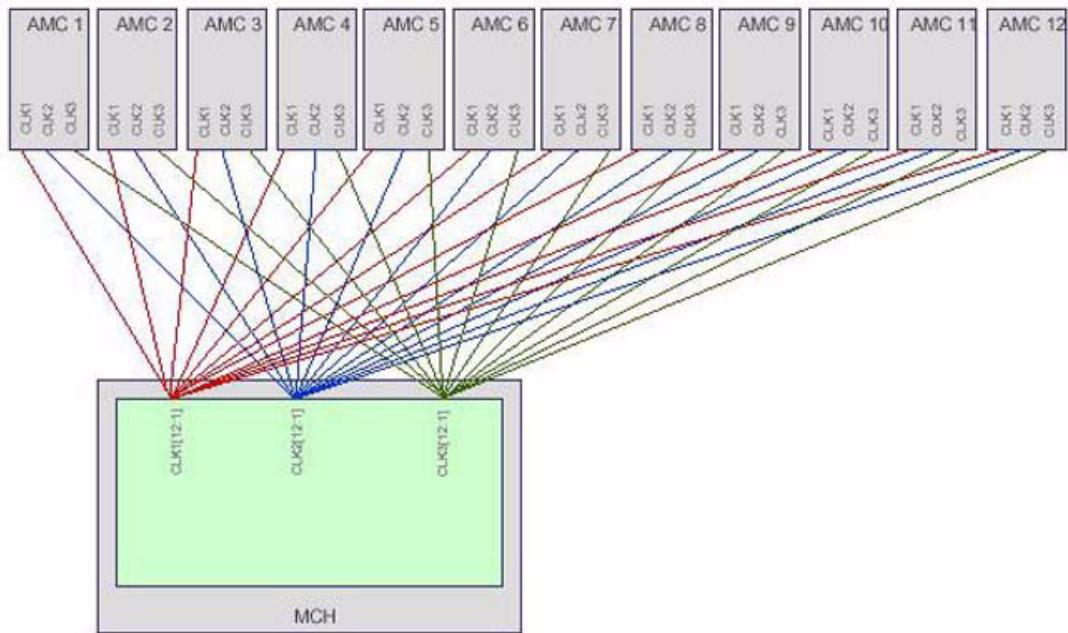


Figure 2.4 Non-Redundant uTCA Clock Architecture

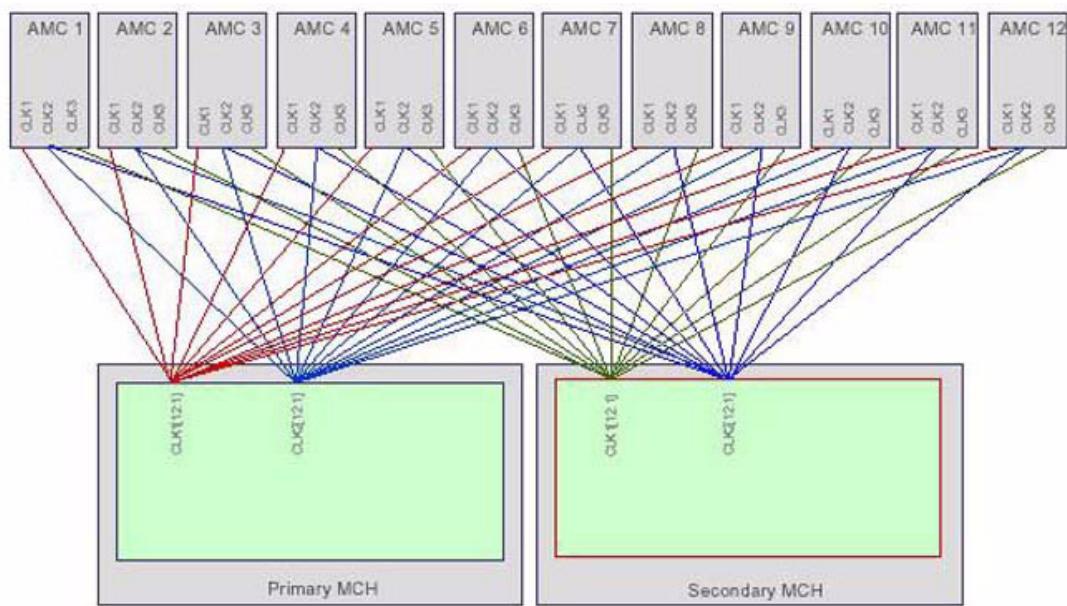


Figure 2.5 Redundant uTCA Clock Architecture

2.4 Common Options

UTCA-5503 connects to each AMC through one channel which consists of a high speed differential transmit and receive pair (Star topology). Receive/transmit cross-over wiring is implemented on the uTCA backplane. Systems utilizing two (redundant) MCH's may be used to implement Dual Star topologies. The Advantech MCH supports a Gigabit Ethernet interface for the common options utilizing a 1000Bx (SERDES) interface to the backplane. Other fabric implementations are not supported. The two MCH's of an uTCA system have a cross connection for the base fabric which may be used for cascading / linking the base fabric switches.

2.5 Fat Pipes

Fat pipes are optional and may be used for any kind of switch fabric interconnects. Each MCH connects to the AMCs with 4 channels each in a Star topology.

Typical fabrics supported are:

- PCIe
- SRIO
- GbE
- XAUI

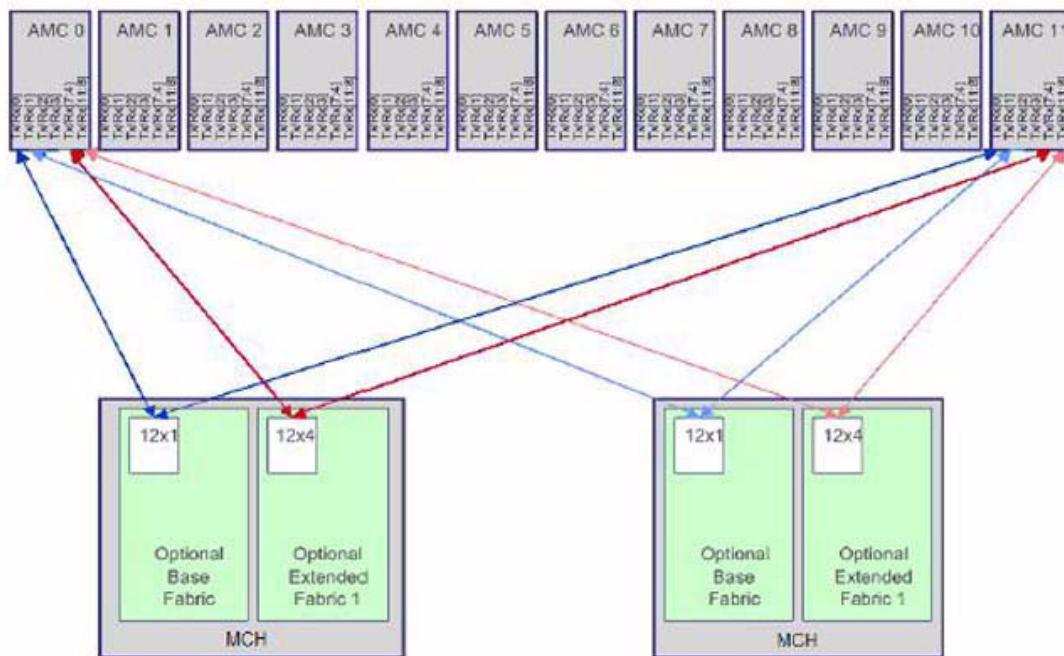


Figure 2.6 Typical uTCA Fabric Architecture

Chapter 3

Mezzanine Module Options

As a modularized MCH base board (PCB1), UTCA-5503 can be completed with additional functionalities by integrating with mezzanine PCB's such as PCB2, PCB3, and PCB4. These PCB's are mounted like a stack and share one common face plate. This chapter will delve into more detail about the integration of these mezzanine PCB's with UTCA-5503.

3.1 PCB Levels and Stacking

Each level may have access to a backplane connector. This interface may be implemented with a standard, AMC-style card edge connector or an MCH tongue ("plug") connector. The aMCH uses card edge connectors for PCB Levels 1 and 2 and plug connectors for PCB Levels 3 and 4. The board-to-board interconnection is allowed for the following PCB levels.

- PCB1 to PCB2
- PCB1 to PCB3
- PCB3 to PCB4

All PCBs of the aMCH need to implement a thickness of 1.6mm +/-10%. The maximum PCB outline is described in detail in the MicroTCA base specification including the card edge and tongue connector details.

3.2 Base Module (PCB1)

As mentioned in the previous chapters, the aMCH base module carries, (1) an IPMI controller for up to twelve AMC modules, Power and Cooling Units, backplane devices, and front panel connectors, and (2) two GbE Layer2 switches for Fabric A for up to twelve AMC modules, front panel uplink, and SGMII interface for the CPU/L3 switch on PCB3. See Figure 3.1 and Table 3.1 for detailed description of the base module.

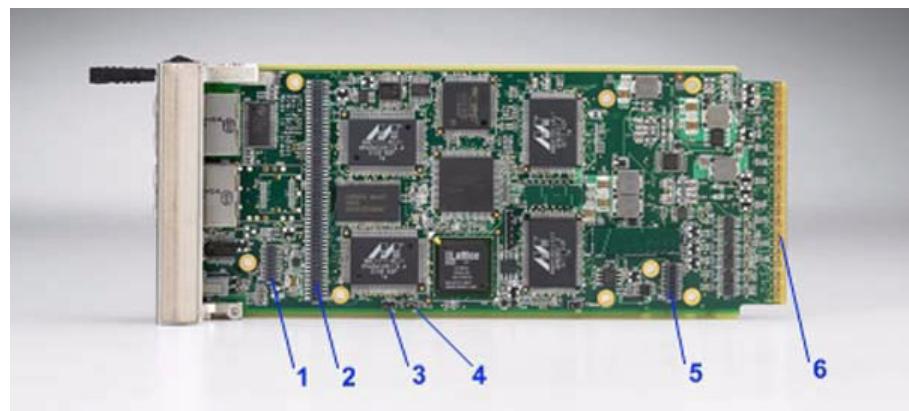


Figure 3.1 Base Module PCB View

Table 3.1: Base Module Connection and Jump Headers

	Silk Screen	Description
1	CN8	Clock/Alarm module header (for future use)
2	CN5	PCB3 module header (for future use)
3	CN12	Mini USB debug console default mode after power up - it is possible to switch between both interfaces at runtime. Open = select H8S serial debug interface. Closed = select H8S command line interface
4	CN13	LAN1 routing control jumper. Open = routed to management LAN. Closed = routed to GbE switches
5	CN9	PCB2 module header (for future use)
6		AMC card edge connector

3.3 Clock Module and Clock IO/Alarm Module (PCB2)

PCB2 can consist of two mezzanines - a Clock IO/Alarm Module and a Clock Module (see Figure 3.2). The Clock IO/Alarm Module contains the interfaces or ports for multi-carrier/shelf clock distribution and synchronization (daisy chain cabling supported) as well as external reference clock receptions such as GPS derived clocks, BITS clocks, or other general purpose clocks. Up to two SMA connectors can be implemented on the front panel of the module. The Clock Module can be designed with various clock generator options for synchronous network system applications such as distribution of accurate timing at Stratum 2 from Stratum 1, Stratum 3 from Stratum 2, or Stratum 4 from Stratum 2/3. In addition, it can provide clock transmitters/receivers, multiplexers, and routing functionalities for the AMC modules, the other MCH, and the Clock IO/Alarm Module. Two high-speed differential clocks can be interfaced between the Clock Module and PCB3 (fabric switch) with the input being driven by PCB3 and the output being driven by the Clock Module. Fabric clock delivered to the AMC's or vice versa is interfaced through the Clock Module. Fabric clock delivered to "the outside" world is also interfaced through the Clock Module with the Clock IO/Alarm Module working as the output.

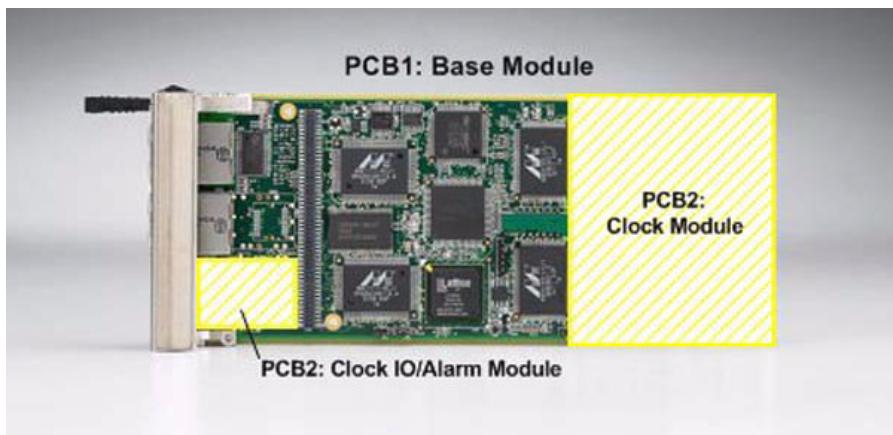


Figure 3.2 Illustration of PCB2 location relative to PCB1

3.4 Fabric Extension Module (PCB3)

PCB3 is a fabric extension module of MCH PCB1. Its purpose is to provide fat pipes switching capabilities for PCIe protocol. Each MCH connects to the AMCs with 4 channels each in a Star topology and to the second MCH with 4 channels. Such logic is considered to be in the payload domain. E-keying is implemented by I2C configuration bus connected on the MCMC through a buffer. There are two high speed differential clocks connecting to the Clock Module to support high speed clock distribution, especially in spread spectrum environments. PCB3 will implement a MCH tongue 3 and 4 connector to reduce the mating force for the MCH. See Figure 3.3 for illustration. The PCIe switch based PCB3 for UTCA-5503 is called UTCA-5533.

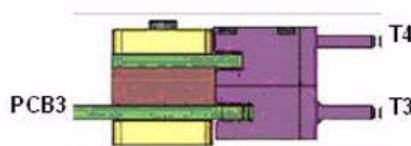


Figure 3.3 Connection between Tongue 3 and Tongue 4 (Yamaichi MCH plug)

3.5 Additional Fabric Extension Module (PCB4)

PCB4 also serves as a fabric extension module of PCB1. However, the actual dimensions and limitations of the module will heavily depend on the PCB3 implementation. So, PCB3 and PCB4 should always be considered as a common set.

3.6 Front Panel Connectors and Indicators

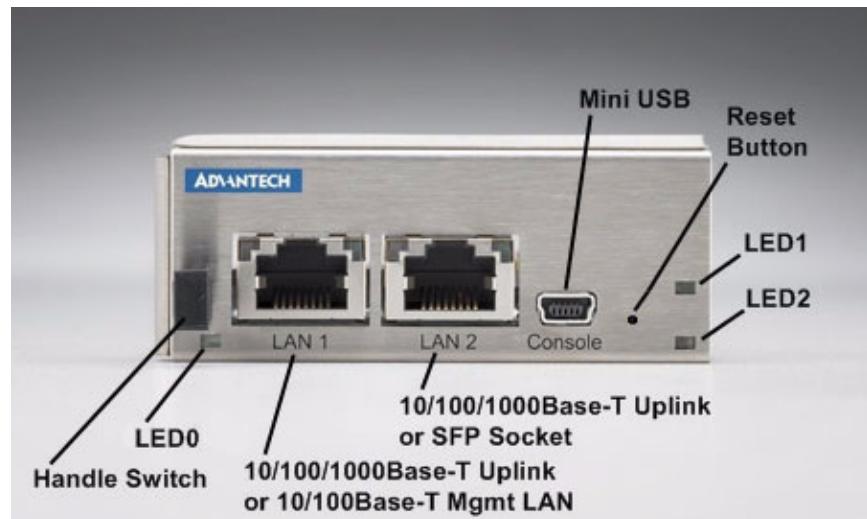


Figure 3.4 UTCA-5503 Front Panel

3.6.1 MCMC LED Indicators

Although the uTCA specification still mandates four LEDs, UTCA-5503 implementation follows the latest AMC.0 specification.

Table 3.2: Front Panel MCMC LED's

LED	Color	Description
0	Blue	Hot swap indicator
1	Red	Flashing = Bootloader active or update (FW/FPGA) running; application temporarily out of service Solid = OOS (error)
2	Green	Flashing = FW application active (payload unpowered) Solid = FW application active (payload powered)

3.6.2 Handle Switch

A handle switch is implemented to support the hot swap function of the MCMC. The handle switch type and location are designed according to the MicroTCA base specification.

3.6.3 Mini USB

The USB port is used for debugging, diagnostic information and implementation of a serial console interface.

3.6.4 Reset Button

The reset button at the front panel is used for resetting the MCMC.

3.6.5 LAN1

A low profile RJ45 connector with integrated LED's and transformer is used for LAN1. It can be used for 10/100/1000Base-T uplink or 10/100Base-T management LAN connection.

3.6.6 LAN2

By default, LAN2 also uses a low profile RJ45 connector with integrated LED's and transformer. It's used for 10/100/1000Base-T connection. However, as a product option, an SFF INF80741 compliant SFP module connector and card cage can be implemented to replace the RJ45 port.

Chapter 4

Operations

4.1 Power the MCH

4.1.1 Preparation

UTCA-5503 requires an uTCA chassis with uTCA power supply for operation.

4.1.2 Insertion

Insert UTCA-5503 into a MCH slot (PCB1) on the backplane of an uTCA chassis. The chassis can be powered or un-powered as the MCH supports hot swap. When the system is powered and the handle switch is closed, the blue LED (LED0) will start to give long blinks, and the FRU LED2 starts blinking green (FW is active) The blue LED will turn off at the same time. In case of a failure, the red OOS LED will be lit and the FW will constantly reboot, trying a successful startup. LED2 will not be lit on OOS status.

Once the MCH has reached M4 and the payload is powered, LED2 will be permanently lit. When management LAN is routed to the GbE switches, the payload will be powered regardless of the FRU state.

The boot process can be observed through the serial debug interface (chapter 3.2.2).

4.1.3 Extraction

To remove the MCH from the backplane, pull the handle switch - the MCH will start deactivation, and the LED0 will give short blue blinks. When the blue LED is constantly lit, it is safe to extract the MCH.

Additionally LED2 will provide feedback about the payload power status.

4.2 Use Mini-USB Debug Interface

A PC and a USB cable (with regular Type-A plug and Mini-USB Type-A plug) are needed to establish the communication with the MCH's debug interface. The Mini-USB jack allows connecting the H8S debug interface and the command line interface as well as connectivity to PCB3.

4.2.1 Preparation

The Mini-USB debug interface utilizes a Silicon Laboratories CP2102 USB-to-UART bridge. Drivers for Microsoft Windows, Linux, or Mac OS can be found at:

http://www.silabs.com/tgwWebApp/public/web_content/products/Microcontrollers/USB/en/mcu_vcp.htm

Microsoft Windows

After installing the driver and connecting the MCH Mini-USB jack, the CP210x USB-to-UART Bridge Controller can be found in the Windows' Device Manager.

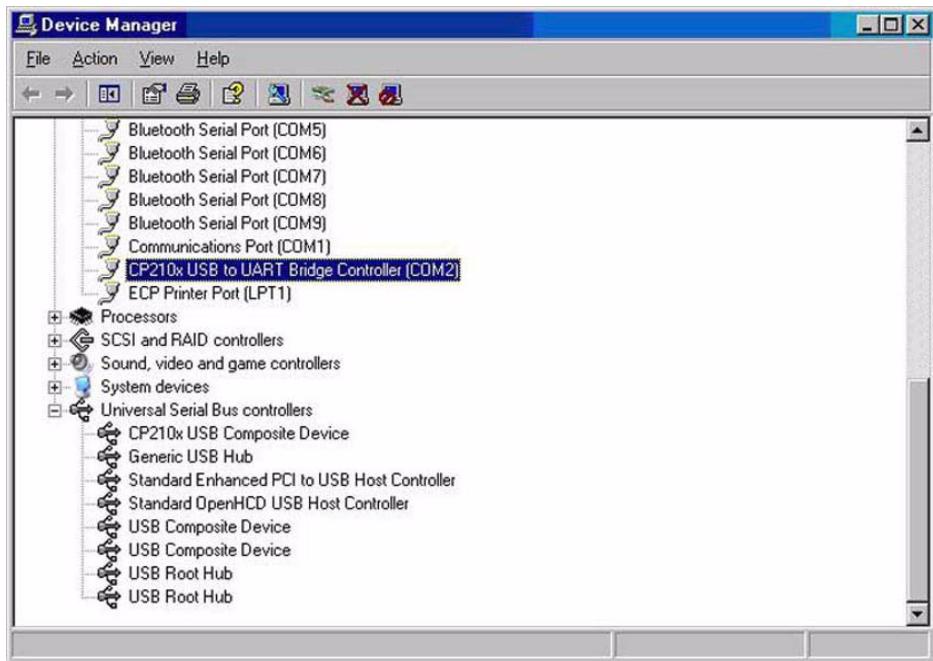


Figure 4.1 USB-to-UART Bridge Controller Shown on Windows' Device Manager

Linux

"`dmesg | grep cp21`" will show if the driver has been loaded successfully. It is included in most of the standard 2.6 kernel Linux distributions.

The screenshot shows a terminal window with the command `dmesg | grep cp21` running. The output shows multiple entries of the CP2101 converter being detected and disconnected from the ttyUSB0 port. A red oval highlights the line "cp2101 1-6:1.0: cp2101 converter detected" which appears twice in the log. The terminal prompt is `boehme@VM-DEBIAN:~$`.

```
boehme@VM-DEBIAN: ~
cp2101 ttyUSB0: cp2101_set_config - Unable to send request, request=0x0 size=2 r
esult=-19
cp2101 ttyUSB0: cp2101 converter now disconnected from ttyUSB0
cp2101 1-6:1.0: cp2101 converter detected
usb 1-6: cp2101 converter now attached to ttyUSB0
cp2101 1-6:1.0: device disconnected
cp2101 ttyUSB0: cp2101_set_config - Unable to send request, request=0x0 size=2 r
esult=-19
cp2101 ttyUSB0: cp2101 converter now disconnected from ttyUSB0
cp2101 1-6:1.0: cp2101 converter detected
usb 1-6: cp2101 converter now attached to ttyUSB0
cp2101 ttyUSB0: cp2101 converter now disconnected from ttyUSB0
cp2101 1-6:1.0: device disconnected
cp2101 1-6:1.0: cp2101 converter detected
usb 1-6: cp2101 converter now attached to ttyUSB0
cp2101 ttyUSB0: cp2101 converter now disconnected from ttyUSB0
cp2101 1-6:1.0: device disconnected
cp2101 1-6:1.0: cp2101 converter detected
usb 1-6: cp2101 converter now attached to ttyUSB0
cp2101 1-6:1.0: device disconnected
cp2101 ttyUSB0: cp2101_set_config - Unable to send request, request=0x0 size=2 r
esult=-19
cp2101 ttyUSB0: cp2101 converter now disconnected from ttyUSB0
boehme@VM-DEBIAN:~$
```

Figure 4.2 cp2101 converter detected when Linux driver installed successfully

4.2.2 Usage

To access the H8S debug interface, set the CN12 jumper (see Table 3.1) to open position and connect the Mini-USB jack to a PC. Open a serial terminal program like HyperTerminal, Putty or Minicom.

RS232 settings: 8N1, 115200 Baud, HW flow control (serial port as seen in the Device Manager on Windows or seen via “dmesg” on Linux).

Note!

 *The USB-to-UART bridge is programmed in such a way that the user can select any baud rate, and the connection will still function at 115200 bits per second.*

If the hardware and driver are set up and installed correctly, the MCH will generate a log like the following during boot-up.

```
BMR-H8S Boot Loader. (c) Pigeon Point Systems.
Advantech aMCH (c) 2007 by Advantech
Exiting the Boot Loader
Running additional POST and custom code.

LAN1: Management LAN routed to base fabric, LAN1 connecting to GbE
switch.

<_>: BMR-H8S Firmware (v1.0.0), MCMC edition.
<_>: Pigeon Point Systems (c) Copyright 2004-2007.
<_>: Advantech aMCH (c) 2007 by Advantech
<_>: Build date: Apr 14 2008 17:08:31

<_>: Reset type: hard, reset cause: power failure
<_>: Operating mode: normal
<_>: E-Keying links disabled
<E>: Setting RTC with the default date

<_>: Initializing Cooling Subsystem
<_>: MCH geographic address: UUU
<_>: MCH site number: 1
<_>: MCH FRU state: M1

<_>: reading and parsing Carrier FRU info
<_>: Partition Table record was found
<_>: found partition #00: 0x0000 - 0x0FFF
<_>: found partition #01: 0x1000 - 0x1FFF
<_>: Carrier IP Link record was found
<_>: This record is ignored, will use Shelf Manager IP address
record
<_>: Carrier Information record was found
<_>: Carrier Number: 1
<_>: 15 sites are defined in Carrier Information record
<_>: found site: CU # 1
<_>: found site: PM # 1
<_>: found site: MCH # 1
<_>: found site: AMC # 1
<_>: found site: AMC # 2
<_>: found site: AMC # 3
<_>: found site: AMC # 4
<_>: found site: AMC # 5
```

```
<_>:    found site: AMC # 6
<_>:    found site: AMC # 7
<_>:    found site: AMC # 8
<_>:    found site: AMC # 9
<_>:    found site: MCH # 2
<_>:    found site: PM # 2
<_>:    found site: CU # 2
<_>:    Carrier Power Policy record was found
<_>:        found PM #1 (role: primary)
<_>:        found PM #2 (role: standby)
<_>:    Carrier Activation and Power Management record was found
<_>:        allowance for module activation readiness: 5
<_>:        PM # 1 auto activation = 01 auto deactivation = 01, power-
on delay = 0.0s, max site current = 0.0A
<_>:        PM # 2 auto activation = 01 auto deactivation = 01, power-
on delay = 0.0s, max site current = 0.0A
<_>:        CU # 1 auto activation = 01 auto deactivation = 01, power-
on delay = 0.0s, max site current = 7.0A
<_>:        CU # 2 auto activation = 01 auto deactivation = 01, power-
on delay = 0.0s, max site current = 7.0A
<_>:        MCH # 1 auto activation = 01 auto deactivation = 01, power-
on delay = 0.0s, max site current = 7.0A
<_>:        MCH # 2 auto activation = 01 auto deactivation = 01, power-
on delay = 0.0s, max site current = 7.0A
<_>:        AMC # 1 auto activation = 01 auto deactivation = 01, power-
on delay = 0.0s, max site current = 7.0A
<_>:        AMC # 2 auto activation = 01 auto deactivation = 01, power-
on delay = 0.0s, max site current = 7.0A
<_>:        AMC # 3 auto activation = 01 auto deactivation = 01, power-
on delay = 0.0s, max site current = 7.0A
<_>:        AMC # 4 auto activation = 01 auto deactivation = 01, power-
on delay = 0.0s, max site current = 7.0A
<_>:        AMC # 5 auto activation = 01 auto deactivation = 01, power-
on delay = 0.0s, max site current = 7.0A
<_>:        AMC # 6 auto activation = 01 auto deactivation = 01, power-
on delay = 0.0s, max site current = 7.0A
<_>:        AMC # 7 auto activation = 01 auto deactivation = 01, power-
on delay = 0.0s, max site current = 7.0A
<_>:        AMC # 8 auto activation = 01 auto deactivation = 01, power-
on delay = 0.0s, max site current = 7.0A
<_>:        AMC # 9 auto activation = 01 auto deactivation = 01, power-
on delay = 0.0s, max site current = 7.0A
<_>:    Shelf Manager Fan Geography record found
<_>:        CU # 1:  AMC # 1  AMC # 2  AMC # 3  AMC # 4  AMC # 5  AMC # 6
<_>:        CU # 1:  AMC # 7  AMC # 8  AMC # 9  CU # 1  CU # 2  PM # 1
<_>:        CU # 1:  PM # 2  MCH # 1  MCH # 2
<_>:        CU # 2:  AMC # 1  AMC # 2  AMC # 3  AMC # 4  AMC # 5  AMC # 6
<_>:        CU # 2:  AMC # 7  AMC # 8  AMC # 9  CU # 1  CU # 2  PM # 1
<_>:        CU # 2:  PM # 2  MCH # 1  MCH # 2
<_>:    found a Carrier Point-to-Point Connectivity record
<_>:    Shelf Manager IP address record was found
<_>:        Shelf Manager #1 IP address: 172.21.35.102
<_>:        Subnet #1 mask: 255.255.255.0
<_>:        Gateway #1 IP address: 0.0.0.0
<_>:        Shelf Manager #2 IP address: 172.21.35.108
<_>:        Subnet #2 mask: 255.255.255.0
<_>:        Gateway #2 IP address: 0.0.0.0
```



```
<_>: found 1 working PM(s)
<_>: Inserted modules:
<_>:   CU # 1
<_>:   PM # 1
<_>:   MCH # 1
<_>: Current power distribution:
<_>:   PM # 1 feeds as primary (used 4.0A):
<_>:     MCH # 1 (M,P,E)
<_>:     CU # 1 (M,P,E)
<_>: Event from CM Sensor #0 "Hot Swap CM"
<_>: Event from CM Sensor #0 "Hot Swap CM"
<_>: Event from CM Sensor #13 "Hot Swap CU 1"
<_>: Event from CM Sensor #15 "Hot Swap PM 1"
<_>: Event from CM Sensor #19 "Hot Swap MCH 1"
<_>: Event from CM Sensor #19 "Hot Swap MCH 1"
<_>: Event from CM Sensor #27 "IPMB Physical"
<_>: MCH FRU state: M3->M4, cause = 0
<_>: Event from ShM Sensor #0 "Hot Swap ShMM": raw 04 F0 00 6F A4 03
00
<_>: Event from CM Sensor #0 "Hot Swap CM"
<_>: Event from CM Sensor #19 "Hot Swap MCH 1"
<_>: Allowance for FRU activation readiness expired
```

4.3 Use Command Line Interface

Keep the same hardware setup as before (chapter 4.1), the Mini-USB jack allows connecting the command line interface.

4.3.1 Usage

To access the H8 command line interface to the uShM, set the CN12 jumper (see Table 3.1) to short position. Serial interface parameters are the same as for serial debug interface (8N1, 115200, HW flow control).

It is also possible to switch to the Command Line Interface by issuing the command [cli] in the serial debug console. To return to the serial debug console, type “exit” in the Command Line Interface.

After booting up the MCH, type “help” at the prompt. All available commands will be shown as illustrated in the following.

```
Pigeon Point MicroTCA Shelf Manager ver. 1.0.0
Pigeon Point is a trademark of Pigeon Point Systems.
Copyright (c) 2002-2007 Pigeon Point Systems
Advantech aMCH (c) 2007 by Advantech
Build date/time: Apr 14 2008 17:08:23
All rights reserved

cli> help
  fru [ipmc [fru]]
  deactivate ipmc fru
  activate ipmc fru
  frudata ipmc fru offset data1 [data2...data22]
  frudata [ipmc [fru]]
  exit
  sendmod fruid netfn cmd data1 [data2...data17]
  sendcmd addr netfn cmd data1 [data2...data25]
  upgrade
  date [YYYY MM DD hh mm [ss] | hh mm [ss]]
  version
  ipmc [ipmc]
  sensordata [ipmc [[lun:]number]]
  sensor [ipmc [[lun:]number]]
  cooling policy [on|off]
  shelf fs
  shelf fans_state
  shelf cs
  shelf cooling_state
  fans [fru]
  alarm [minor|major|critical|clear]
  sel clear [ipmc]
  sel info [ipmc]
  sel [-v] [ipmc [record_count [starting_record]]]
cli>
```

Figure 4.3 Available MCH Commands

4.4 LAN

The MCH has 2 front panel RJ45 jacks (see Figure 3.4). LAN1 is 10/100/1000Mb capable when it is routed to the GbE switches. However, it is 10/100 Mb capable when routed to the management LAN controller. LAN2 is 10/100/1000Mb capable.

4.4.1 Preparation

To use the GbE capability of LAN1, a GbE capable counter-part such as GbE NIC or GbE switch connection is required. For direct access to the management LAN controller via LAN1, a crossover patch cable is needed. If the management LAN is routed through the GbE switch fabric, both straight as well as crossover cables can be used as the GbE switches support auto-crossover.

To access the MCH via Ethernet, appropriate LAN addresses must be configured.

If the operator does not know the shelf manager's IP address, it can be found in the serial (Mini-USB) debug output as illustrated in the following.

```
<_>: Shelf Manager IP address record was found
<_>: Shelf Manager #1 IP address: 172.21.35.102
<_>: Subnet #1 mask: 255.255.255.0
<_>: Gateway #1 IP address: 0.0.0.0
<_>: Shelf Manager #2 IP address: 172.21.35.108
<_>: Subnet #2 mask: 255.255.255.0
<_>: Gateway #2 IP address: 0.0.0.0
<_>: Actual Shelf Manager IP address is 172.21.35.102
<_>: Actual gateway IP address is 172.21.35.102
<_>: Actual subnetwork mask is 255.255.255.0
```

Figure 4.4 Illustration of Shelf Manager's IP Address

As shown in Figure 4.4, the shelf manager's IP address is 192.168.16.17. If necessary the counter-part NIC can be configured with an available fixed IP address in the same subnet, for example 192.168.16.30.

4.4.2 Usage

4.4.2.1 LAN1 routed directly to management LAN controller

Jumper CN13 (see Table 3.1) should be set to the open position. LAN1 is now routed directly to the management LAN controller. In this configuration LAN1 is only 10/100 Mb capable. To connect LAN1 directly to a PC NIC, a crossover patch cable must be used.

4.4.2.2 LAN1 routed to switch

Jumper CN13 should be set to the closed position. LAN1 is now routed to the GbE switch (and is 10/100/1000 Mb capable). The management LAN controller is now connected to the switch. In this configuration it doesn't matter if a crossover or a normal patch cable is used as the GbE switches support auto-crossover.

4.4.2.3 LAN2

LAN2 is always connected to the switch. It is also 10/100/1000 Mb capable. A normal as well as crossover patch Ethernet cables can be used on LAN2 because the GbE switches support auto-crossover.

4.5 MCMC/MCH Management Subsystem

The MCMC/MCH Management Subsystem is a firmware component that implements the MicroTCA functionality related to exposing the MCMC and MCH resources to the Shelf/System Managers. This subsystem is responsible for handling the IPMI/PICMG commands related to the MCMC/MCH resources, implementing MCMC/MCH sensor devices and exposing MCMC/MCH FRU devices.

The MCMC exposes two FRU devices. The first FRU device (as a logical module) represents the Carrier Manager function and is exposed as FRU device #0. The second FRU device represents the MCH as a physical module and its resources, including the MCMC-controlled LEDs, the Hot Swap switch of the MCH, and the MCH payload. This FRU device is exposed as FRU device #3 or #4, depending on the slot in which the MCH is installed.

In addition, the MCMC registers one FRU device for each AMC/PM/CU site implemented in the carrier and controlled by the Carrier Manager. The FRU devices representing the managed modules have numbers defined by the MTCA.0 Specification (i.e. 4-15 for AMCs, 40-41 for CUs, and 50-53 for PMs).

The MCMC/MCH FRU devices and managed module FRU devices are treated differently by the MCMC firmware. In particular, all IPMI/PICMG commands targeting the MCMC/MCH FRUs, as well as some specific IPMI/PICMG commands targeting the FRU devices representing the managed modules (e.g. the Set FRU Activation command), are handled by the MCMC itself. However, some of the commands targeting the FRU devices representing the managed modules, such as the FRU Device commands, are just forwarded to the respective module over the IPMB-0 or IPMB-L interface. For such commands, the MCMC implements transparent forwarding of responses back to the interfaces from which they arrive.

Additionally, the MCMC firmware implements the event receiver functionality for the IPMB-0 and IPMB-L interfaces as required by the MTCA Specifications. That is, the MCMC is capable of receiving events from the managed modules and forwarding them to the uShM over the IP-based Shelf-Carrier Manager interface.

4.5.1 MCMC operation with external uTCA Shelf Manager

The UTCA-5503 firmware implements both Carrier Manager and Shelf Manager and currently does not support the use of external Shelf Managers.

4.5.2 Commands supported by the MCMC

Please refer to Appendix B for a list of commands supported by the MCMC.

4.6 uSHM Subsystem

Both Carrier Manager and uTCA Shelf Manager are implemented as modular software blocks running on the same CPU. They are connected to each other through a virtual IPMB channel, thus allowing both software components to behave like physically separated Carrier Manager and uTCA Shelf Manager.

The uShM implements mandatory functionality as defined in the ATCA Specification (SDR Repository, System Event Log) as well as some optional functionality (Platform Event Filtering, Cooling Policy).

4.6.1 **RMCP Module**

UTCA-5503 provides access to the uShM through the IPMI-defined RMCP protocol (refer to section 12 of the IPMI Specification). This IP-based interface allows external RMCP-capable System Management Tools (e.g. OpenIPMI or OpenHPI with ipmidirect Plugin) to interact with the MCH.

The uShM's RMCP interface supports message bridging, therefore it is possible to communicate with the CM/MCMC as well as FRUs located on the IPMB-0 or IPMB-L buses through this connection.

4.6.2 **Cooling Policy**

The UTCA-5503 uShM implements a fixed standard cooling policy to control the fans in the chassis, using a simple yet effective mechanism based on events and time-outs.

The uShM constantly monitors all temperature sensors in the shelf as well as the fan speed sensors of each cooling unit. If there are no active events for a specified time, the uShM will gradually reduce the speed of all fans down to the minimum speed level defined for each cooling unit.

Any event reporting that a sensor in the system has crossed one of the upper limits will gradually increase fan speed until that sensor will deassert the event. After a specific timeout the uShM will then again begin to gradually reduce fan RPM.

Critical temperature events or events from fan speed sensors (indicating fan failure) will cause the uShM to immediately set all fans to maximum RPM in order to compensate for any potential issues.

Chapter 5

Firmware Upgrades

5.1 MCMC Boot Process

Located at the beginning of the user memory space of the H8S processor is a small software component called the boot loader, which has several important tasks to perform for the MCMC boot process. The MCMC firmware is also located at the user memory space, right behind the boot loader. A second copy is held in external flash, providing roll back features in case of failed FW upgrades.

The MCMC boot process will include the following steps:

1. The Boot Loader performs an early Power-On Self Test (POST) of the hardware.
2. The Boot Loader calculates the checksum of the MCMC firmware image. If the checksum is not valid, the Boot Loader sends a notification message to the Serial Debug line and enters the upgrade mode.
3. The Boot Loader checks if the most recent reset was caused by a user upgrade request received by the MCMC firmware from a serial interface. If so, the Boot Loader sends a notification message to the Serial Debug line and enters the upgrade mode.
4. Optionally, the Boot Loader polls the Serial Debug Interface for an amount of time and if an ESC (ASCII 27) character is read from this interface before this time elapses, the Boot Loader sends a notification message to the Serial Debug line and enters the upgrade mode.
5. If the Boot Loader is in the normal (not upgrade mode), it passes control to the MCMC firmware by calling its entry point.

The following self tests are performed in POST:

- H8S internal SRAM test (read/write)
- FPGA status and register access test
- External SRAM test
- FRU EEPROMs
- SDRs
- I2C device access

A failing FPGA test is a critical error of the aMCH. The MCMC will turn on the OOS LED and try to re-program the FPGA from the recovery image programmed during the manufacturing process. It will then trigger a board reset and try to restart.

5.2 MCMC Firmware Validation

In addition to the MCMC firmware being located in the user memory space in H8S, a backup copy of the MCMC firmware is also stored in an external flash memory. As mentioned in the previous section, the Boot Loader will perform a checksum operation to validate the MCMC firmware (in H8S) during boot up. If the checksum operation fails, the firmware image is judged as non-functional. The Boot Loader will then restore the firmware from the backup copy.

Each time when the MCMC firmware is upgraded via the Boot Loader, a redundant copy of the current firmware is saved in the external flash first followed by downloading and programming the new image to H8S. If the firmware upgrade is interrupted (e.g. a power failure occurs) or the new firmware turns out to be corrupted, the Boot Loader will also restore the backup image from the external flash.

5.3 Upgrading MCMC Firmware

If a UTCA-5503 board needs a firmware upgrade, for example, there is a new firmware release called “upgrade.img”, the following simple steps can be taken to program the MCMC.

1. Follow Section 4 for system and debug preparations.
2. Power up the UTCA-5503 board.
3. If the current FW fails to start up, instantly hit the ESC key after power on to stop the MCH in bootloader mode. Else wait until FW has finished the boot process.
4. Close terminal window.
5. Open a DOS window and change to the file directory that contains “upgradefw.exe” (available for download under the “Firmware” tab on the “Downloads” section of UTCA-5503 product page on Advantech’s website) and the new firmware “upgrade.img”. Note: upgradefw is also available in a Linux version
6. Enter the following command at the prompt.
`upgradefw -s com2:115200 upgrade.img`

Note!

HPM.1 support and other update channels (LAN, I2C) will be available in future firmware releases.



com2 is a place holder and needs to be replaced with the actual COM port of the CP2102 is using

The command line for Linux is “./upgradefw -s /dev/ttyUSB:115200 upgrade.img” with the USB0 once again being the actual CP2102 device.

5.4 FPGA Firmware Download/Upgrade Process

The FPGA firmware has similar upgrade policy as the MCMC’s. The external flash holds a fixed FPGA recovery image that is being programmed during manufacturing, allowing recovery of the FPGA if there are any problems. In case of FPGA POST problems, this image will automatically be restored and the MCH will restart.

New firmware can be downloaded to the FPGA through a second image in external flash that can be updated by the user, using a specific tool as described below. This update will run in the background, the new FPGA configuration will only become active after a power cycle.

In case of a download failure (e.g. power interruption during FPGA upgrade), the MCMC firmware will automatically restore the FPGA contents from the recovery image upon the next firmware start-up.

5.5 Upgrading FPGA Firmware

If a UTCA-5503 board needs a FPGA firmware upgrade, for example, there is a new firmware release called “fpgaupgrade.img”, the following steps can be taken to program the FPGA.

1. Follow Section 4 for system and debug preparations.
2. Power up the UTCA-5503 board.
3. Wait until the FW has fully booted up
4. Close terminal window.
5. Open a DOS window and change to the file directory that contains “upgradefpga.exe” (available for download under the “Firmware” tab on the “Downloads” section of UTCA-5503 product page on Advantech’s website) and the new firmware “fpgaupgrade.img”. Note: upgradefpga is also available in a Linux version
6. Enter the following command at the prompt.

```
upgradefpga -s com2:115200 fpgaupgrade.img
```

Note! *HPM.1 support and other update channels (LAN, I2C) will be available in future firmware releases.*



com2 is a place holder and needs to be replaced with the actual COM port of the CP2102 is using

The command line for Linux is “./upgradefw -s /dev/ttyUSB:115200 upgrade.img” with the USB0 once again being the actual CP2102 device.

Chapter 6

**Overview of
Supported Features
and Known
Limitations**

Below is a list of UTCA-5503's current supported and unsupported features.

MCMC firmware version: 01.00, FPGA firmware version: 01.00

Table 6.1: Current supported and unsupported features

Feature	Supported	Unsupported	REMARK
Carrier Manager basic features (FRU access, message bridging, sensor events and alerts, e-Keying)	✓		
Shelf Manager (uShM) basic features (AMC detection, activation, deactivation)	✓		
Power Budgeting	✓		
System Event Log (SEL) with RTC	✓		
Sensor Data Repository (SDR)	✓		
Platform Event Filtering (PEF)	✓		
Cooling Policy	✓		
Serial Debug Interface routed to mini-USB	✓		
Management LAN routing directly to front port	✓		
Management LAN routing though GbE fabric	✓		
RMC connections to uShM	✓		
PPS specific FW update (SDI, CLI)	✓		
Redundant FW (backup copy in external flash)	✓		
Switch fabric e-Keying	✓		
Switch fabric Front Port connection	✓		
Switch fabric backplane update channel	✓		
Switch fabric to AMC connection	✓		
External system manager connection	✓		
External shelf manager	✓		Not supported in combination with integrated uShM
Redundant MCH (uShM)	✓		Not yet supported by PPS
HPM.1 update	✓		Not yet supported by PPS; working in progress
FPGA update through HPM.1	✓		Work in progress
FW/FPGA update through IPMB/Management LAN	✓		Not yet supported by PPS
Redundant Power Module	✓		
Dual Cooling Unit	✓		

Known Limitations:

Current MCMC Firmware does not support redundant MCH configurations. Insertion of two MCHs may have unpredictable results and is explicitly prohibited.

Appendix **A**

**MCH Pin List,
Connector 1**

A.1 MCH Pin List, Connector 1

Table A.1: MCH Pin List, Connector 1

Pin No.	Signal	Pin No.	Signal
85	GND	86	GND
84	PWR	87	IPMBL-SDA-12
83	PS0#	88	IPMBL-SCL-12
82	GND	89	GND
81	XOVER2-	90	IPMBL-SDA-11
80	XOVER2+	91	IPMBL-SCL-11
79	GND	92	GND
78	XOVER1-	93	IPMBL-SDA-10
77	XOVER1+	94	IPMBL-SCL-10
76	GND	95	GND
75	XOVER0-	96	IPMBL-SDA-9
74	XOVER0+	97	IPMBL-SCL-9
73	GND	98	GND
72	PWR	99	IPMBL-SDA-8
71	SDL_L	100	IPMBL-SCL-8
70	GND	101	GND
69	RxFA-12-	102	IPMBL-SDA-7
68	RxFA-12+	103	IPMBL-SCL-7
67	GND	104	GND
66	TxFA-12-	105	IPMBL-SDA-6
65	TxFA-12+	106	IPMBL-SCL-6
64	GND	107	GND
63	RxFA-12-	108	IPMBL-SDA-5
62	RxFA-12+	109	IPMBL-SCL-5
61	GND	110	GND
60	TxFA-11-	111	IPMBL-SDA-4
59	TxFA-11+	112	IPMBL-SCL-4
58	GND	113	GND
57	PWR	114	IPMBL-SDA-3
56	SCL_L	115	IPMBL-SCL-3
55	GND	116	GND
54	RxFA-10-	117	IPMBL-SDA-2
53	RxFA-10+	118	IPMBL-SCL-2
52	GND	119	GND
51	TxFA-10-	120	IPMBL-SDA-1
50	TxFA-10+	121	IPMBL-SCL-1
49	GND	122	GND
48	RxFA-9-	123	IPMB0-SDA-B
47	RxFA-9+	124	IPMB0-SCL-B
46	GND	125	GND
45	TxFA-9-	126	IPMB0-SDA-A
44	TxFA-9+	127	IPMB0-SCL-A
43	GND	128	GND

Table A.1: MCH Pin List, Connector 1

42	PWR	129	I2C_SDA
41	ENABLE#	130	I2C_SCL
40	GND	131	GND
39	RxFA-7-	132	RSVD
38	RxFA-7+	133	TMREQ#
37	GND	134	GND
36	TxFA-7-	135	RxFA-8-
35	TxFA-7+	136	RxFA-8+
34	GND	137	GND
33	RxFA-5-	138	TxFA-8-
32	RxFA-5+	139	TxFA-8+
31	GND	140	GND
30	TxFA-5-	141	RxFA-6-
29	TxFA-5+	142	RxFA-6+
28	GND	143	GND
27	PWR	144	TxFA-6-
26	GA2	145	TxFA-6+
25	GND	146	GND
24	RxFA-3-	147	RxFA-4-
23	RxFA-3+	148	RxFA-4+
22	GND	149	GND
21	TxFA-3-	150	TxFA-4-
20	TxFA-3+	151	TxFA-4+
19	GND	152	GND
18	PWR	153	RxFA-2-
17	GA1	154	RxFA-2+
16	GND	155	GND
15	RxFUA-	156	TxFA-2-
14	RxFUA+	157	TxFA-2+
13	GND	158	GND
12	TxFUA-	159	RxFA-1-
11	TxFUA+	160	RxFA-1+
10	GND	161	GND
9	PWR	162	TxFA-1-
8	RSVD	163	TxFA-1+
7	GND	164	GND
6	RSVD	165	TCK
5	GA0	166	TMS
4	MP	167	TRST#
3	PS1#	168	TDO
2	PWR	169	TDI
1	GND	170	PWR_ON

Appendix **B**

**IPMI/PICMG Command
Subset Supported by
the MCMC**

B.1 IPMI/PICMG Command Subset Supported by the MCMC

Table B.1: IPMI/PICMG Command Subset Supported by the MCMC

Command	IPMI/ATCA/ AMC/MTCA Spec	NetFn	CMD	Carrier Manager Req
IPMI Device “Global” Commands				
Get Device ID	17.1	App	01h	Mandatory
Cold Reset	17.2	App	02h	Optional
Warm reset	17.3	App	03h	Optional
Get Self Test Results	17.4	App	04h	Mandatory
Get Device GUID	17.8	App	08h	Optional
IPMI Messaging Support Commands				
Set BMC Global Enables	18.1	App	2Eh	Mandatory
Get BMC Global Enables	18.2	App	2Fh	Mandatory
Clear Message Flags	18.3	App	30h	Mandatory
Get Message Flags	18.4	App	31h	Mandatory
Get Message	18.6	App	33h	Mandatory
Send Message	18.7	App	34h	Mandatory
Master Write-Read	18.10	App	52h	Optional
Get Channel Authentication Capabilities	18.12	App	38h	Mandatory
Get Session Challenge	18.14	App	39h	Mandatory
Activate Session	18.15	App	3Ah	Mandatory
Set Session Privilege Level	18.16	App	3Bh	Mandatory
Close Session	18.17	App	3Ch	Mandatory
Get Session Info	18.18	App	3Dh	Mandatory
Set Channel Access	18.20	App	40h	Mandatory
Get Channel Access	18.21	App	41h	Mandatory
Get Channel Info	18.22	App	42h	Mandatory
Set User Access	18.23	App	43h	Mandatory
Get User Access	18.24	App	44h	Mandatory
Set User Name	18.25	App	45h	Mandatory
Get User Name	18.26	App	46h	Mandatory
Set User Password	18.27	App	47h	Mandatory
BMC Watchdog Timer				
Reset Watchdog Timer	21.5	App	22h	Mandatory
Set Watchdog Timer	21.6	App	24h	Mandatory
Get Watchdog Timer	21.7	App	25h	Mandatory
Event Commands				
Set Event Receiver	23.1	S/E	00h	Mandatory
Get Event Receiver	23.2	S/E	01h	Mandatory
Platform Event	23.3	S/E	02h	Mandatory
Sensor Device Commands				
Get Device SDR Info	29.2	S/E	20h	Mandatory
Get Device SDR	29.3	S/E	21h	Mandatory

Table B.1: IPMI/PICMG Command Subset Supported by the MCMC				
Reserve Device SDR Repository	29.4	S/E	22h	Mandatory
Set Sensor Hysteresis	29.6	S/E	24h	Optional
Get Sensor Hysteresis	29.7	S/E	25h	Optional
Set Sensor Threshold	29.8	S/E	26h	Optional
Get Sensor Threshold	29.9	S/E	27h	Optional
Set Sensor Event Enable	29.10	S/E	28h	Optional
Get Sensor Event Enable	29.11	S/E	29h	Optional
Rearm Sensor Events	29.12	S/E	2Ah	Optional
Get Sensor Event Status	29.13	S/E	2Bh	Optional
Get Sensor Reading	29.14	S/E	2Dh	Mandatory
FRU Device Commands				
Get FRU Inventory Area Info	28.1	Storage	10h	Mandatory
Read FRU Data	28.2	Storage	11h	Mandatory
Write FRU Data	28.3	Storage	12h	Mandatory
LAN Device Commands				
Get LAN Configuration Parameters	19.1	Transport	01h	Mandatory
Set LAN Configuration Parameters	19.2	Transport	02h	Mandatory
AdvancedTCA Commands				
Get PICMG Properties	3-10	PICMG	00h	Mandatory
Get Address Info	3-9	PICMG	01h	Mandatory
FRU Control	3-25	PICMG	04h	Mandatory
Get FRU LED Properties	3-27	PICMG	05h	Mandatory
Get LED Color Capabilities	3-28	PICMG	06h	Mandatory
Set FRU LED State	3-29	PICMG	07h	Mandatory
Get FRU LED State	3-30	PICMG	08h	Mandatory
Set IPMB State	3-65	PICMG	09h	Mandatory
Set FRU Activation Policy	3-19	PICMG	0Ah	Mandatory
Get FRU Activation Policy	3-20	PICMG	0Bh	Mandatory
Set FRU Activation	3-18	PICMG	0Ch	Mandatory
Get Device Locator Record ID	3-35	PICMG	0Dh	Mandatory
Set Power Level	3-79	PICMG	11h	Mandatory
Get Fan Speed Properties	3-81	PICMG	14h	Mandatory
Set Fan Level	3-83	PICMG	15h	Mandatory
Get Fan Level	3-82	PICMG	16h	Mandatory
Get IPMB Link Info	3-63	PICMG	18h	Mandatory
FRU Control Capabilities	3-24	PICMG	1Eh	Mandatory
MicroTCA Commands				
Get Telco Alarm Capability	3-39	PICMG	23h	Mandatory
Set Telco Alarm	3-40	PICMG	24h	Mandatory
Get Telco Alarm State	3-41	PICMG	25h	Mandatory

Appendix C

**IPMI/PICMG Command
Subset Supported by
the Carrier Manager**

C.1 IPMI/PICMG Command Subset Supported by the Carrier Manager

Table C.1: IPMI/PICMG Command Subset Supported by the Carrier Manager

Command	IPMI/PICMG/ AMC/MTCA Spec	NetFn	CMD	Carrier Manager Req
IPM Device “Global” Commands				
Get Device ID	17.1	App	01h	Mandatory
Broadcast “Get Device ID”	17.9	App	01h	Mandatory
Event Commands				
Platform Event	23.3	S/E	02h	Mandatory
Sensor Device Commands				
Get Device SDR Info	29.2	S/E	20h	Mandatory
Get Device SDR	29.3	S/E	21h	Mandatory
Reserve Device SDR Repository	29.4	S/E	22h	Mandatory
Get Sensor Reading Factors	29.5	S/E	23h	Optional
Set Sensor Hysteresis	29.6	S/E	24h	Optional
Get Sensor Hysteresis	29.7	S/E	25h	Optional
Set Sensor Threshold	29.8	S/E	26h	Optional
Get Sensor Threshold	29.9	S/E	27h	Optional
Set Sensor Event Enable	29.10	S/E	28h	Optional
Get Sensor Event Enable	29.11	S/E	29h	Optional
Rearm Sensor Events	29.12	S/E	2Ah	Optional
Get Sensor Event Status	29.13	S/E	2Bh	Optional
Get Sensor Reading	29.14	S/E	2Dh	Mandatory
FRU Device Commands				
Get FRU Inventory Area Info	28.1	Storage	10h	Mandatory
Read FRU Data	28.2	Storage	11h	Mandatory
Write FRU Data	28.3	Storage	12h	Mandatory
AdvancedTCA Commands				
Get PICMG Properties	3-10	PICMG	00h	Mandatory
FRU Control	3-25	PICMG	04h	Mandatory
Get FRU LED Properties	3-27	PICMG	05h	Mandatory
Get LED Color Capabilities	3-28	PICMG	06h	Mandatory
Set FRU LED State	3-29	PICMG	07h	Mandatory
Get FRU LED State	3-30	PICMG	08h	Mandatory
Get Device Locator Record ID	3-35	PICMG	0Dh	Mandatory
Get Fan Speed Properties	3-81	PICMG	14h	Mandatory
Set Fan Level	3-83	PICMG	15h	Mandatory
Get Fan Level	3-82	PICMG	16h	Mandatory
FRU Control Capabilities	3-24	PICMG	1Eh	Mandatory
AMC Commands				
Set AMC Port State	3-26	PICMG	19h	Mandatory
Get AMC Port State	3-27	PICMG	1Ah	Mandatory
MicroTCA Commands				

Table C.1: IPMI/PICMG Command Subset Supported by the Carrier Manager

Power Channel Control	3-28	PICMG	24h	Mandatory
Get Power Channel Status	3-29	PICMG	25h	Mandatory
PM Reset	3-31	PICMG	26h	Mandatory
Get PM Status	3-32	PICMG	27h	Mandatory
PM Heartbeat	3-33	PICMG	28h	Mandatory
Get Telco Alarm Capability	3-40	PICMG	29h	Mandatory
Set Telco Alarm	3-41	PICMG	2Ah	Mandatory
Get Telco Alarm State	3-42	PICMG	2Bh	Mandatory

Appendix **D**

**IPMI/PICMG Command
Subset Supported by
the uShM**

D.1 IPMI/PICMG Command Subset Supported by the uShM

Table D.1: IPMI/PICMG Command Subset Supported by the uShM

Command	IPMI Spec	NetFn	CMD	MTCA.0 Req
IPMI Device “Global” Commands				
Get Device ID	17.1	App	01h	Mandatory
Cold Reset	17.2	App	02h	Optional
Warm Reset	17.3	App	03h	Optional
Get Self Test Results	17.4	App	04h	Mandatory
Get Device GUID	17.8	App	08h	Optional
BMC Device and Messaging Support Commands				
Send Message	18.7	App	34h	Mandatory
Get System GUID	18.13	App	37h	Optional
Get Channel Authentication Capabilities	18.12	App	38h	Mandatory
Get Session Challenge	18.14	App	39h	Mandatory
Activate Session	18.15	App	3Ah	Mandatory
Set Session Privilege Level	18.16	App	3Bh	Mandatory
Close Session	18.17	App	3Ch	Mandatory
Get Session Info	18.18	App	3Dh	Mandatory
Set Channel Access	18.20	App	40h	Mandatory
Get Channel Access	18.21	App	41h	Mandatory
Get Channel Info	18.22	App	42h	Mandatory
Set User Access	18.23	App	43h	Mandatory
Get User Access	18.24	App	44h	Mandatory
Set User Name	18.25	App	45h	Mandatory
Get User Name	18.26	App	46h	Mandatory
Set User Password	18.27	App	47h	Mandatory
Event Commands				
Platform Event	23.3	S/E	02h	Mandatory
PEF and Alerting Commands				
Get PEF Capabilities	24.1	S/E	10h	Mandatory
Set PEF Configuration Parameters	24.3	S/E	12h	Mandatory
Get PEF Configuration Parameters	24.4	S/E	13h	Mandatory
Set Last Processed Event ID	24.5	S/E	14h	Mandatory
Get Last Processed Event ID	24.6	S/E	15h	Mandatory
PET Acknowledge	24.8	S/E	17h	Optional
Sensor Device Commands				
Get Device SDR Info	29.2	S/E	20h	Mandatory
Get Device SDR	29.3	S/E	21h	Mandatory
Reserve Device SDR Repository	29.4	S/E	22h	Mandatory
Get Sensor Reading Factors	29.5	S/E	23h	Optional
Set Sensor Hysteresis	29.6	S/E	24h	Optional
Get Sensor Hysteresis	29.7	S/E	25h	Optional
Set Sensor Threshold	29.8	S/E	26h	Optional
Get Sensor Threshold	29.9	S/E	27h	Optional

Table D.1: IPMI/PICMG Command Subset Supported by the uShM				
Set Sensor Event Enable	29.10	S/E	28h	Optional
Get Sensor Event Enable	29.11	S/E	29h	Optional
Get Sensor Event Status	29.13	S/E	2Bh	Optional
Get Sensor Reading	29.14	S/E	2Dh	Mandatory
FRU Device Commands				
Get FRU Inventory Area Info	28.1	Storage	10h	Mandatory
Read FRU	28.2	Storage	11h	Mandatory
Write FRU	28.3	Storage	12h	Mandatory
SDR Device Commands				
Get SDR Repository Info	27.9	Storage	20h	Mandatory
Reserve SDR Repository	27.11	Storage	22h	Mandatory
Get SDR	27.12	Storage	23h	Mandatory
Add SDR	27.13	Storage	24h	Mandatory
Partial Add SDR	27.14	Storage	25h	Mandatory
Delete SDR	27.15	Storage	26h	Optional
Clear SDR Repository	27.16	Storage	27h	Mandatory
Enter SDR Repository Update Mode	27.19	Storage	2Ah	Optional
Exit SDR Repository Update Mode	27.20	Storage	2Bh	Mandatory
SEL Device Commands				
Get SEL Info	25.2	Storage	40h	Mandatory
Get SEL Entry	25.5	Storage	43h	Mandatory
Add SEL Entry	25.6	Storage	44h	Mandatory
Clear SEL	25.9	Storage	47h	Mandatory
Get SEL Time	25.10	Storage	48h	Mandatory
Set SEL Time	25.11	Storage	49h	Mandatory
Reserve SEL	25.4	Storage	42h	Optional
LAN Device Commands				
Get LAN Configuration Parameters	19.1	Transport	01h	Mandatory
Set LAN Configuration Parameters	19.2	Transport	02h	Mandatory
AdvancedTCA				
Get PICMG Properties	3-9	PICMG	00h	Mandatory
Get Address Info	3-8	PICMG	01h	Mandatory
FRU Control	3-21	PICMG	04h	Optional
Get FRU LED Properties	3-23	PICMG	05h	Mandatory
Get LED Color Capabilities	3-24	PICMG	06h	Mandatory
Set FRU LED State	3-25	PICMG	07h	Mandatory
Get FRU LED State	3-26	PICMG	08h	Mandatory
Set FRU Activation Policy	3-16	PICMG	0Ah	Mandatory
Get FRU Activation Policy	3-17	PICMG	0Bh	Mandatory
Set FRU Activation	3-15	PICMG	0Ch	Mandatory
Get Device Locator Record ID	3-28	PICMG	0Dh	Mandatory
FRU Control Capabilities	3-24	PICMG	1Eh	Mandatory

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